Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.200”**

**.200”**

**E**

**B**

**Top Material: Al**

**Backside Material: Ti Ni Ag**

**Bond Pad Size: .0036”**

**Backside Potential: Collector**

**Mask Ref: 008201**

**APPROVED BY: DK DIE SIZE .200” X .200” DATE: 11/17/21**

**MFG: ON SEMI / MOTOROLA THICKNESS .014” P/N: 2N6287**

**DG 10.1.2**

#### Rev B, 7/19/02